CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a charge pump circuit comprising a plurality of charge pump cascades, each of the charge pump cascades comprising a plurality of pump stages; and

wherein the plurality of charge pump cascades are driven to pump charge to a common output in response to alternate edges of a system clock signal.

2. The semiconductor device of claim 1, further comprising a non-overlapping clock signal generator, the non-overlapping clock signal generator generating non-overlapping clock signals in response to alternate rising and falling edges of the system clock signal.

3. The semiconductor device of claim 1, wherein the common output provides an output supply voltage that is greater than a power supply voltage provided to the charge pump circuit.

4. A memory device including a charge pump circuit comprising:

a first and second charge pump cascade, the first and second charge pump cascade comprising a plurality of charge pump stages;

each of the plurality of charge pump stages comprising a transistor and a capacitor; and

wherein the plurality of charge pump stages pump charge to an output node on both a rising edge and a falling edge of a system clock signal.

5. The memory device of claim 4, wherein the transistor comprises a PFET configured as a diode.

6. The memory device of claim 4, wherein the capacitor comprises a PFET configured as a capacitor.

7. The memory device of claim 4, wherein the first and second charge pump cascades receive a power supply voltage and are in communication with the output node and wherein the output node provides an output supply voltage that is greater than the power supply voltage.

8. The memory device of claim 4, further comprising a non-overlapping clock signal generator for generating a first and a second phase signal in response to opposite phases of the system clock signal wherein the first phase signal drives (2n)th charge pump stage of the first charge pump cascade and (2n +1)th charge pump stage of the second charge pump cascade and wherein the second phase signal drives (2n + 1)th charge pump stage of the first charge pump cascade and (2n)th charge pump stage of the second charge pump cascade, n being an integer greater than or equal to zero.

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9. A charge pump comprising:

a first and a second pump cascade coupled in parallel to an output node;

the first and the second pump cascades comprising a plurality of pump stages coupled in series;

wherein (2n)th pump stage of the first pump cascade is coupled to receive a first clock signal and (2n+1)th pump stage of the first pump cascade is coupled to receive a second clock signal, n being an integer greater than or equal to zero;

wherein (2n)th pump stage of the second pump cascade is coupled to receive the second clock signal and (2n +1)th pump stage of the second pump

cascade is coupled to receive the first clock signal, n being an integer greater than or equal to zero; and

wherein the output node receives charge pumped by the first and the second pump cascades and provides an output supply voltage that is greater in magnitude than the power supply voltage.

10. The charge pump of claim 9, wherein each pump stage comprises a PFET configured as a diode and a PFET configured as a capacitor.

11. The charge pump of claim 9, wherein a first pump stage of each of the first and second pump cascades comprises a thin oxide PFET configured as a diode and a thin oxide PFET configured as a capacitor.

12. A charge pump for generating a high voltage supply comprising:

a first pump cascade comprising multiple charge pump stages, each charge pump stage in the first pump cascade being driven by a first plurality of clock signals;

a second pump cascade comprising multiple charge pumps stages, each charge pump stage in the second pump cascade being driving by a second plurality of clock signals;

a non-overlapping clock signal generator for generating the first and second plurality of clock signals in response to transitions in a system clock signal, each

of the clock signals of the second plurality of clock signals having opposite phases to each of the clock signals of the first plurality of clock signals; and

wherein final charge pump stages of the first and second pump cascades are coupled in parallel to provide the high voltage supply.

13. A memory device including a charge pump comprising:

a first and second charge pump cascade, the first and second charge pump cascade comprising a plurality of charge pump stages;

wherein each of the plurality of charge pump stages comprises a means for receiving charge and a means for storing charge; and

means for driving an output node with charge stored in the plurality of charge pump stages on both a rising edge and a falling edge of a system clock signal.

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14. The memory device of claim 13, wherein the means for receiving charge comprises a PFET configured as a diode.

15. The memory device of claim 13, wherein the means for storing charge comprises a PFET configured as a capacitor.

16. The memory device of claim 13, wherein the first and second charge pump cascades are powered by a power supply voltage and are coupled in common to the output node and wherein the output node provides an output supply voltage that is greater than the power supply voltage.

17. The memory device of claim 13, wherein means for driving an output node comprises a first and a second phase signal comprising opposite phases of the system clock signal wherein the first phase signal drives (2n)th charge pump stage of the first charge pump cascade and (2n +1)th charge pump stage of the second charge pump cascade and wherein the second phase signal drives (2n + 1)th charge pump stage of the first charge pump cascade and (2n)th charge pump stage of the second charge pump cascade, n being an integer greater than or equal to zero.

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18. A method for generating a voltage greater than a power supply voltage, comprising the steps of:

providing the power supply voltage to a plurality of pump cascades comprising a plurality of pump stages;

on a first edge of a system clock, storing charge from a power supply simultaneously in a first group of charge pump stages and pumping charge to an output node from a second group of charge pump stages; and

on a second edge of the system clock, storing charge from the power supply simultaneously in the second group of charge pump stages and pumping charge to the output node from the first group of charge pump stages.

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19. A method of operating a plurality of charge pump cascades, each charge pump cascades comprising a first and second group of charge pump stages, and wherein the charge pump cascades operate to pump electrical charge to an output supply node, the method comprising the steps of:

in response to a leading edge of a system clock, pre-charging output nodes of the first group of charge pump stages to voltages present on respective input nodes in the first group of charge pump stages and subsequently boosting output nodes of the second group of charge pump stages to respective boosted voltages;

in response to a trailing edge of the system clock, pre-charging output nodes in the second group of charge pump stages to voltages present on respective input nodes in the second group of charge pump stages and subsequently boosting output nodes in the first group of charge pump stages to respective boosted voltages; and

providing charge in alteration from each of the charge pump cascades to the output supply node in response to both leading and trailing edges of the system clock until the output supply node reaches a predetermined voltage level.

20. A non-overlapping clock signal generator comprising:

a system clock input node;

a clock input stage;

a latch coupled to the clock input stage having intermediate latch outputs and complementary latch outputs;

clock output driving stages coupled to the complementary latch outputs and having non-overlapping clock signal outputs; and

and equalization stage coupled between the clock output driving stages and receiving as inputs the intermediate latch outputs.